AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 3, line 1 with the following amended paragraph:

-- According to the object of the invention, ~~a dynamic random access memory cell layout has a first conductor line pair and a second conductor line pair extending along a first direction, in which each conductor line pair comprises a first conductive line and a second conductive line, and in which each conductive line comprises a gate conductive line portion and a word line portion. A bitline pair has a first bitline and a second bitline, which extend along a second direction and intersect the conductor line pairs. Corresponding to the first bitline, a first active area extends along the second direction to cross the first conductor line pair. Corresponding to the second bitline, a second active area extends along the second direction to cross the second conductor line pair. Each active area has a first deep trench and a second deep trench formed in a substrate underneath the first conductive line and the second conductive line, respectively. A bitline contact is formed between the first conductive line and the second conductive line to be electrically connected to the corresponding bitline. A common source/drain region is formed in the substrate between the first conductive line and the second conductive line to be electrically connected to the bitline contact. A first vertical transistor and a second vertical transistor are formed overlying the first deep trench and the second deep trench, respectively. Each vertical transistor has a buried strap out-diffusion region formed in the substrate adjacent to one sidewall of the deep trench.~~ a transistor has a source/drain region, a buried strap out-diffusion region adjacent to one sidewall of a deep trench and a bended gate. The bended gate has a first portion extending along a first direction and a second portion extending along a second direction intersecting with the first direction. The first portion of the bended gate is adjacent to the source/drain region and the second portion of bended gate is adjacent to the buried strap out-diffusion region.

Please add the following new paragraphs beginning on page 7, line 22:

Stilling referring to FIG. 4, the bended gate 104 (GC_1 or GC_2) has a first portion 106 extending along a first direction 202 and a second portion 108 extending along a second direction 204 intersecting with the first direction 202, wherein the first portion 106 of the bended gate 104 is

adjacent to the source/drain region (S/D) and the second portion 108 of bended gate 104 is adjacent to the buried strap out-diffusion region (BS_1 or BS_2).

The bended gate 104 (GC_1or GC_2) is adjacent to a shallow trench isolation (STI). The first direction 202 is perpendicular to the second direction 204. The first direction 202 is parallel to the surface of substrate 40. The second direction 204 is parallel to a sidewall of the trench (DT_1 or DT_2).

A spacer 102 is formed on a sidewall of the bended gate (GC_1or GC_2) between the bit line contact (BC) and the bended gate (GC_1 or GC_2). The bended gate 104 (GC_1 or GC_2) is L shaped. The bended gate oxide layer 110 underlying the bended gate 104 is also L shaped.